the positive electrode of the capacitor (C_1; C_{1p}) of the associated branch, and the grid of each transistor (M_1; M_{1p}) is connected to the positive electrode of the capacitor (C_1; C_{1p}) and to the source of the transistor in the opposite branch, and in that the negative electrodes of the capacitors (C_1; C_{1p}) are respectively connected to two clock signals (Φ_1; Φ_2) in phase opposition.

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~~5.~~ (currently amended) A converter according to claim 3 ~~or claim~~[[4]], characterized in that the capacitors (C_i; C_{ip}) of the two branches (B_1; B_2) of the voltage multiplier stage have their positive electrodes respectively connected to the outputs of two switches (K_i; K_{ip}) via two nodes (V_i; V_{ip}), and their negative electrodes connected to respective clock signals (Φ_i), in that an input of each switch (K_i; K_{ip}) is connected to the output of the preceding stage, and in that the clock signal (Φ_i) corresponds either to the signal (Φ_1) if [[i]] (i) is odd for the first branch (B_1) and to the signal (Φ_2) if [[i]] (i) is even for the first branch (B_1), or to the signal (Φ_2) if [[i]] (i) is odd for the second branch (B_2) and to (Φ_1) if [[i]] (i) is even for the second branch (B_2).

6. (currently amended) A converter according to ~~any preceding~~ claim 1, characterized in that the control circuit (CC_i) of the voltage multiplier circuit (CM_i) of the first branch (B_1) is an inverter circuit (I_i) which is powered between the voltage (V_{i-1}) from the voltage multiplier circuit of the preceding stage in the first branch (B_1), and the voltage (V_{ip}) from the voltage multiplier circuit of the same stage in the second branch (B_2), and in that the inverter (I_i) is controlled either by the voltage ($V_{c(i-1)}$) of the preceding voltage multiplier circuit of the first branch (B_1) or by the voltage (V_i) from the voltage multiplier circuit (CM_i) of the first branch (B_1).

7. (currently amended) A converter according to ~~any preceding~~ claim 1, characterized in that the control circuit (CC_{ip}) of the voltage multiplier circuit (CM_{ip}) of the second branch (B_2) is an inverter circuit (I_{ip}) which is powered between the output voltage ($V_{(i-1)p}$) of the voltage multiplier circuit ($CM_{(i-1)p}$) of the preceding stage of the second branch (B_2) and the output voltage (V_i) of the voltage multiplier

IN THE CLAIMS:

Please amend claims as follows.

1. (original) A voltage/voltage converter for integrated circuits, the converter presenting a symmetrical multistage structure and comprising at least one input stage constituted by a clock booster circuit (CB) of symmetrical structure which delivers two output voltages, a voltage multiplier circuit of symmetrical structure comprising two voltage multiplier circuits (CM_i; CM_{ip}) respectively connected in two branches (B_1; B_2) of the converter and having the output voltages of the input stage applied respectively thereto, and an output stage (S) constituted by a multiplexer circuit (MX) having the two output voltages from the voltage multiplier stage applied thereto, the converter being characterized in that each voltage multiplier circuit (CM_i; CM_{ip}) is controlled by a control circuit (CC_i; CC_{ip}), and in that each voltage multiplier circuit (CM_i; CM_{ip}) supplies voltages needed both for the operation of its own control circuit and for the operation of the control circuit of the other voltage multiplier circuit of the same stage.

2. (original) A converter according to claim 1, characterized in that the clock booster circuit (CB) serves to add a DC component to a clock signal, and in that the clock booster circuit (CB) comprises two similar circuits receiving respective clock signals (Φ_1; Φ_2) of opposite phase.

3. (currently amended) A converter according to claim 1 ~~or claim 2~~, characterized in that each voltage multiplier circuit (CM_i; CM_{ip}) comprises a capacitor (C_i; C_{ip}) and a switch (K_i; K_{ip}) for controlling charging of the capacitor and transfer of its charge to the voltage multiplier circuit of the following stage.

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4. (currently amended) A converter according to ~~any preceding~~ claim 1, characterized in that it has a positive output, in that the clock booster circuit (CB) forming the input stage has a positive output and comprises two NMOS transistors and two capacitors, in that the drain of each transistor (M_1; M_{1p}) is connected to a power supply terminal (V_{dd}), the source of each transistor (M_1; M_{1p}) is connected to